REMARKS

By this Amendment, claims 1-19 are cancelled, and claims 20-41 are added. Thus, claims 20-41 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

A Notice of Draftperson's Patent Drawing Review form attached to the Office Action indicated that the top margin of Figure 2 was incorrect. Accordingly, replacement formal drawings of Figures 1-6 are submitted herewith under a separate cover letter to correct the identified informalities of Figure 2. Each of the replacement formal drawing sheets are labeled as a "Replacement sheet". Approval of the replacement formal drawings is respectfully requested.

The specification and abstract have been carefully reviewed and revised to grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification.

In item 2 on page 2 of the Office Action, claims 1-2, 8-9 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Miller et al. (U.S. 5,615,270). This rejection is respectfully traversed. Furthermore, the Applicant submits that this rejection is inapplicable to new claims 20-41 for the following reasons.

New claim 20, which has been added in favor of cancelled claim 1, recites an integrating apparatus which comprises a plurality of integrating circuits each operable to integrate an input signal and to output an integrated signal, and an output unit operable to selectively derive an output having a lowest level from among integrated signals output from said plurality of integrating circuits. Furthermore, new claim 20 also recites that the plurality of integrating circuits each have a different fall time constant. New claim 29, which has been added in favor of cancelled claim 8, recites an audio system which comprises the integrating apparatus as recited in new claim 20.

Miller et al. discloses a method and apparatus for dynamic sound optimization (DSO) of sound reproduced by audio systems in vehicles. The DSO system of Miller et al. compensates for noise outside the audio system of the vehicle. The DSO system, which is incorporated into a microprocessor 26, includes an input subsystem 36, a compressor subsystem 38, a decimator subsystem 44, a nuller subsystem 40 and a power estimator subsystem 42. The input subsystem 36 is disclosed as receiving left and right music inputs from the audio system and an input from a microphone 16, which detects a noise level inside the vehicle cabin. The input subsystem 36 filters out lower frequency audio signals which are inaudible to a human ear. The filtered output of the input subsystem 36 is supplied to the compressor subsystem 38 and the decimator subsystem 44.

The compressor subsystem 38 of Miller et al. is disclosed as determining whether the filtered signals output from the input subsystem 36 are increasing or not. The compressor subsystem 38 then adjusts a gain calculator 60 responsive to the determination of whether the filtered signal output from the input subsystem 36 and to a modified noise signal output from the power estimator subsystem, which indicates the actual noise level inside the vehicle cabin (see Column 5, lines 44-60). The compressor subsystem 38 includes a single integrator 66 which integrates the filtered signal output from the input subsystem 36 over time. The integrating time used in the integrator 66 varies according to whether the filtered signals output from the input subsystem 36 are increasing or decreasing (see Column 5, lines 66-67). The integrated filtered signal is held in box 66b and is then provided to a comparator 66a which compares the held integrated filtered signal to a subsequent filtered signal output from the input subsystem 36 so as to determine whether the filtered signals being output from the input subsystem 36 are increasing or not (see Column 6, lines 1-3).

Accordingly, since the compressor subsystem 38 only includes a single integrator 66, the comparator 65 merely compares the integrated filtered signals to subsequent filtered signals output from the input subsystem 36. Therefore, the compressor subsystem of Miller et al. does not disclose or suggest deriving an output having a lowest level from integrated signals output from a plurality of integrating circuits, as recited in new claims 20 and 29. Furthermore, the gain

calculator 60 constantly adjusts the gain calculation responsive to each integrated filtered signal and the modified noise signal output from the power estimator subsystem 42, and thus, the gain calculator also does not disclose or suggest deriving an output having a lowest level from integrated signals output from a plurality of integrating circuits, as recited in new claims 20 and 29.

As described above, the DSO system of Miller et al. also includes a power estimator subsystem 42. The power estimator subsystem 42 receives a noise signal, in which the right and left audio signals have been removed, from the nuller subsystem 40 and a microphone signal from the decimator subsystem 44 (see Column 8, lines 9-12 and Figure 8). In the power estimator subsystem 42, the noise signal output from the nuller subystem 40 is integrated by an integrator 74a, and the microphone signal output from the decimator subsystem 44 is integrated by an integrator 74b. The integrated outputs from the integrators 74a and 74b are compared by a comparator 75. In rejecting claim 1, the Examiner asserted, on page 2 of the Office Action that since the comparator 75 of the power estimator 42 compares the integrated outputs from the integrators 74a and 74b, the comparator "inherently select[s] the low level output amongst the integrating circuits for enabling adequate signal-to-noise ratio". However, as is clearly evident from Figure 8 of Miller et al., the comparator 75 is a subtractor circuit which subtracts the integrated noise signal from the integrated microphone signal so as to determine the compressor SNR influence. That is, the comparator 75 outputs a signal (the compressor SNR influence) indicating the result of the subtraction between the integrated noise signal and the integrated microphone signal. Therefore, the comparator 75 of Miller et al. is clearly not disclosed or suggested as deriving an output having a lowest level from among the integrated signals output from the integrators 74a and 75b. Accordingly, Miller et al. clearly does not disclose or suggest an output unit which is operable to selectively derive an output having a lowest level from among integrated signals output from the plurality of integrating circuits, as recited in new claims 20 and 29.

Therefore, new claims 20 and 29 are clearly not anticipated by Miller et al. since Miller et al. does not disclose each and every limitation as recited in new claims 20 and 29. Accordingly,

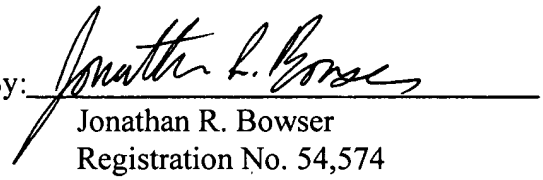
the Applicant respectfully submits that new claims 20 and 29, as well as new claims 21-28 and 30-41 which depend therefrom, are clearly allowable.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

Hiroshi KOWAKI

By: 

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#15 Ex. B.J. 6/3/04

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Attorney Authorization

2. Authorization for this examiner's amendment was given in a telephone interview with Jonathan R. Bowser on May 27, 2004.

Amended Changes

3. The application has been amended as follows:

a) Claims 22-23, 31-32 and 35-36 have been cancelled.

b) Claim 20, line 3, "and" has been deleted.

c) Claim 20, line 3, --, said plurality of integrating circuits each having a different fall time constant -- has been inserted before the ";".

D1

d) Claim 20, line 5, -- and – has been inserted after the ";".

e) Line 6 of claim 20 has been deleted.

f) Claim 20, -- a plurality of first amplifiers operable to amplify the input signal and to output the amplified input signal to said plurality of integrating circuits, respectively; wherein each of said plurality of first amplifiers has an amplification factor corresponding to the fall time constant of a respective one of said plurality

D2

of integrating circuits to which the input signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and

wherein each of said plurality of integrating circuits comprises: an adder operable to add the amplified input signal and a feedback signal, and to output a resultant added signal; a delaying unit operable to delay the resultant added signal and to produce a delayed output signal; and

a second amplifier operable to amplify the delayed output signal and to produce an amplified output signal; and wherein the amplified output signal output from said second amplifier is inputted to said adder as the feedback signal, and the resultant added signal is produced as integrated signal output from said integrating circuit. -- has been inserted after line 5.

g) Claim 29, line 4, --, said plurality of integrating circuits each having a different fall time constant -- has been inserted before the ";".

h) Claim 29, line 8, "and" has been deleted.

i) Line 11 of claim 29 has been deleted.

j) Claim 29, line 10, -- and -- has been inserted after the ";".

k) Claim 29, -- a plurality of first amplifiers operable to amplify the input signal and to output the amplified input signal to said plurality of integrating circuits, respectively; wherein each of said plurality of first amplifiers has an amplification factor corresponding to the fall time constant of a respective one of said plurality of integrating circuits to which the input signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and

wherein each of said plurality of integrating circuits comprises: an adder operable to add the amplified input signal and a feedback signal, and to output a resultant added signal; a delaying unit operable to delay the resultant added signal and to produce a delayed output signal; and

D4 Cont

a second amplifier operable to amplify the delayed output signal and to produce an amplified output signal; and wherein the amplified output signal output from said second amplifier is inputted to said adder as the feedback signal, and the resultant added signal is produced as integrated signal output from said integrating circuit. --has been inserted after line 10.

l) Claim 24, "23" has been deleted and replaced with -- 20 --.

m) Claim 27, "23" has been deleted and replaced with -- 20 --.

n) Claim 33, line 3, "said integrating apparatus according to claim 20" has been deleted.

o) Claim 33, line 3, -- an integrating apparatus -- has been inserted after the comma.

q) Claim 33, line 4, before the ".", -- a plurality of integrating circuits each operable to integrate an input signal and to output an integrated signal, said plurality of integrating circuits each having a different fall time constant; an output unit operable to selectively derive an output having a lowest level from among integrated signals output from said plurality of integrating circuits; and a plurality of first amplifiers operable to amplify the input signal and to output the amplified input signal to said plurality of integrating circuits, respectively; wherein each of said plurality of first amplifiers has an amplification factor corresponding to the

D5

fall time constant of a respective one of said plurality of integrating circuits to which the input signal is inputted such that the amplification factor is larger when the fall time constant is smaller; and wherein each of said plurality of integrating circuits comprises an adder operable to add the amplified input signal arid a feedback signal, and to output a resultant added signal, a delaying unit operable to delay the resultant added signal and to produce a delayed output signal, and a second amplifier operable to amplify the delayed output signal and to produce ate amplified output signal, wherein the amplified output signal output from said second amplifier is inputted to said adder as the feedback signal, and the resultant added signal is produced as the integrated signal output from said integrating circuit -- has been inserted.

D5 cont

r) Claims 34, and 37-40, repectively, line 1, "A" has been deleted and replaced with -- The --.

s) Claims 34, and 37-40, respectively, lines, 2-3 have been deleted.

t) Claims 34, and 37-40, respectively, line 1, "comprising:" has been deleted.

u) Claim 34, after line 1, -- according to claim 10, wherein said plurality of integrating circuits are each controlled so that an average value of the output levels becomes higher as the fall time constant becomes smaller. -- has been inserted.

D6

v) Claim 37, after line 1, -- according to claim 10, wherein said second amplifier has a gain of less than one. -- has been inserted.

D7

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1

w) Claim 38, after line 1, -- according to claim ~~37~~ 12, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling intervals. -- has been inserted.

x) Claim 39, after line 1, -- according to claim ~~38~~ 13, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals. -- has been inserted.

y) Claim 40, after line 1, -- according to claim ~~33~~ 10, wherein said adder is operable to sample and compute the integrated signal at predetermined sampling time intervals. -- has been inserted.

z) Claim 41, after line 1, -- according to claim ~~40~~ 15, wherein said delaying unit is operable to delay the integrated signal on a timescale of the predetermined sampling time intervals. -- has been inserted.

Allowable Subject Matter

4. **Claims 20-21, 24-30, 33-34, and 37-41** are allowed.

5. The following is an examiner's statement of reasons for allowance:

Regarding claim 20, the prior art of record is drawn to integrating means in respect to noise reduction comprising a plurality of integrating circuits, an output means, and the integrating circuits have different fall times. However, the prior art of record fails to specifically disclose or fairly suggest the integrating circuit comprising a plurality of first amplifiers, and second amplifier, an adder, delay unit, therein as claimed.

Regarding claim 29, the prior art of record is drawn to integrating means in respect to noise reduction comprising a plurality of integrating circuits, an output means, and the integrating circuits have different fall times, detecting unit (microphone), an audio source, and attenuation means (compressor). However, the prior art of record fails to specifically disclose or fairly suggest the integrating circuit comprising a plurality of first amplifiers, and second amplifier, an adder, delay unit, therein as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura A Grier whose telephone number is (703) 306-4819. The examiner can normally be reached on Monday - Friday, 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

LAG
May 27, 2004

XU MEI
PRIMARY EXAMINER